09/936,962

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

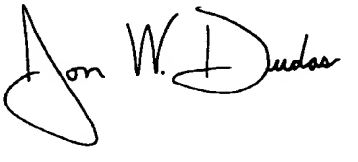
PATENT NO. : 6,788,546 B1
DATED : September 7, 2004
INVENTOR(S) : Phillipe Steiert et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title page,
Item [57], **ABSTRACT,** replace with the following:
-- A multi-chip-module includes a base carrier on which signal conductor tracks and signal contact surfaces arranged at least in a single layer are located, and with a semiconductor component operating in the signal range and connected with the signal conductor track and signal contact surfaces. A high degree of integration is achieved with a multi-chip-module of this type. In some areas on the base carrier power conductor tracks and power contact surfaces arranged in at least one layer are located. Furthermore, at least one power electronics component, operating in the power range, is provided, which is connected with at least one power conductor track, at least one power contact surface and at least one signal conductor track. The power conductor tracks have a larger cross section than the signal conductor tracks at least on the basis of greater thickness dimensions. --

Signed and Sealed this

First Day of February, 2005



JON W. DUDAS
Director of the United States Patent and Trademark Office